

CLAIMS

We claim:

1. A method for making a semiconductor device, comprising:

providing a substrate with an upper surface, the substrate having a trench therein;

providing an oxide layer on the bottom and sidewall of the trench;

providing a conductive layer on the bottom and sidewall of the oxide layer, the

conductive layer having an upper surface below the upper surface of the substrate; and

providing a self-aligned isolation cap on the conductive layer within the trench, the

isolation cap comprising a non-organic dielectric material.

2. The method of claim 1, wherein the isolation cap comprises silicon oxide.

3. The method of claim 1, including providing the isolation cap by providing a first dielectric layer, providing a second dielectric layer over the first dielectric layer, flowing the second dielectric layer, and then anisotropically etching the first and second dielectric layers until the upper substrate surface is exposed.

4. The method of claim 3, including reflowing the second dielectric layer until the upper surface of the second dielectric layer is substantially planar.

5. The method of claim 1, wherein the conductive layer comprises polysilicon or metal.

6. A method for making a semiconductor device, comprising:

providing a substrate with an upper surface, the substrate having a trench therein;

providing an oxide layer on the bottom and sidewall of the trench;

providing a conductive layer on the bottom and sidewall of the oxide layer, the

conductive layer having an upper surface below the upper surface of the substrate; and

providing a self-aligned isolation cap on the conductive layer within the trench by using a combination of dielectric materials with different etching rates.

7. The method of claim 6, including providing the isolation cap by providing a first dielectric layer having a first etching rate in the trench and on the upper substrate surface, providing a second dielectric layer have a etching rate faster than the first etching rate on the first dielectric layer, reflowing the first and second dielectric layers, and then isotropically etching until the upper substrate surface is exposed.

8. The method of claim 7, including reflowing the first and second dielectric layers until the upper surface of the second dielectric layer is substantially planar.

9. The method of claim 7, wherein the first dielectric layer dielectric material comprises PSG, BPSG, or a low-temperature oxide.

10. The method of claim 7, wherein the second dielectric layer dielectric material comprises PSG or BPSG.

11. The method of claim 7, wherein the conductive layer comprises polysilicon or metal.

12. A method for making a semiconductor device, comprising:

providing a substrate with an upper surface;

providing a nitride-containing layer on a portion of the substrate upper surface;

providing a trench in the substrate in the portion of the substrate not containing the nitride-containing layer;

providing an oxide layer on the bottom and sidewall of the trench;

providing a conductive layer on the bottom and sidewall of the oxide layer, the conductive layer having an upper surface below the upper surface of the substrate;

providing a self-aligned isolation cap on the conductive layer within the trench; and
removing the nitride-containing layer.

13. The method of claim 12, the distance between the upper surface of the conductive
layer and the substrate upper surface being about 0.5 microns.

14. The method of claim 12, the conductive layer being polysilicon.

15. The method of claim 14, including providing the isolation cap by oxidizing the upper
surface of the polysilicon layer.

16. The method of claim 12, including providing the isolation cap by selectively
depositing a dielectric layer on the upper surface of the polysilicon layer.

17. The method of claim 12, wherein the conductive layer comprises polysilicon or
metal.

18. A semiconductor device made by the method comprising:
providing a substrate with an upper surface, the substrate having a trench therein;
providing an oxide layer on the bottom and sidewall of the trench;
providing a conductive layer on the bottom and sidewall of the oxide layer, the
conductive layer having an upper surface below the upper surface of the substrate; and
providing a self-aligned isolation cap on the conductive layer within the trench, the
isolation cap comprising a non-organic dielectric material.

19. A semiconductor device made by the method comprising:

providing a substrate with an upper surface, the substrate having a trench therein;
providing an oxide layer on the bottom and sidewall of the trench;

providing a conductive layer on the bottom and sidewall of the oxide layer, the conductive layer having an upper surface below the upper surface of the substrate; and providing a self-aligned isolation cap on the conductive layer within the trench by using a combination of dielectric materials with different etching rates.

20. A semiconductor device made by the method comprising:

providing a substrate with an upper surface;
providing a nitride-containing layer on a portion of the substrate upper surface;
providing a trench in the substrate in the portion of the substrate not containing the nitride-containing layer;
providing an oxide layer on the bottom and sidewall of the trench;
providing a conductive layer on the bottom and sidewall of the oxide layer, the conductive layer having an upper surface below the upper surface of the substrate;
providing a self-aligned isolation cap on the conductive layer within the trench; and removing the nitride-containing layer.

21. A method for making a MOSFET, comprising:

providing a substrate with an upper surface, the substrate having a trench therein;
providing source and channel regions proximate the trench;
providing a gate oxide on the bottom and sidewall of the trench;
providing a conductive gate on the bottom and sidewall of the gate oxide, the conductive gate having an upper surface below the upper surface of the substrate; and providing a self-aligned isolation cap on the conductive gate within the trench, the isolation cap comprising a non-organic dielectric material.

22. A method for making a MOSFET, comprising:

providing a substrate with an upper surface, the substrate having a trench therein;

providing source and channel regions proximate the trench;

providing a gate oxide on the bottom and sidewall of the trench;

providing a conductive gate on the bottom and sidewall of the gate oxide, the conductive

gate having an upper surface below the upper surface of the substrate; and

providing a self-aligned isolation cap on the conductive gate within the trench by using a combination of dielectric materials with different etching rates.

23. The method of claim 22 including providing the isolation cap by providing a first dielectric layer having a first etching rate in the trench and on the upper substrate surface, providing a second dielectric layer have a etching rate faster than the first etching rate on the first dielectric layer, reflowing the first and second dielectric layers, and then isotropically etching until the upper substrate surface is exposed.

24. A method for making a MOSFET, comprising:

providing a substrate with an upper surface;

providing source and channel regions proximate the trench;

providing a nitride-containing layer on a portion of the substrate upper surface;

providing a trench in the substrate in the portion of the substrate not containing the nitride-containing layer;

providing a gate oxide on the bottom and sidewall of the trench;

providing a conductive gate on the bottom and sidewall of the gate oxide, the conductive gate having an upper surface below the upper surface of the substrate;

providing a self-aligned isolation cap on the conductive gate within the trench; and
removing the nitride-containing layer.

25. A MOSFET made by the method comprising:

providing a substrate with an upper surface, the substrate having a trench therein;
providing source and channel regions proximate the trench;
providing a gate oxide on the bottom and sidewall of the trench;
providing a conductive gate on the bottom and sidewall of the gate oxide, the conductive
gate having an upper surface below the upper surface of the substrate; and
providing a self-aligned isolation cap on the conductive layer within the trench, the
isolation cap comprising a non-organic dielectric material

26. A MOSFET made by the method comprising:

providing a substrate with an upper surface, the substrate having a trench therein;
providing source and channel regions proximate the trench;
providing a gate oxide on the bottom and sidewall of the trench;
providing a conductive gate on the bottom and sidewall of the gate oxide, the conductive
gate having an upper surface below the upper surface of the substrate; and
providing a self-aligned isolation cap on the conductive gate within the trench by using a
combination of dielectric materials with different etching rates.

27. A MOSFET made by the method comprising:

providing a substrate with an upper surface;
providing source and channel regions proximate the trench;
providing a nitride-containing layer on a portion of the substrate upper surface;

providing a trench in the substrate in the portion of the substrate not containing the nitride-containing layer;

providing a gate oxide on the bottom and sidewall of the trench;

providing a conductive gate on the bottom and sidewall of the gate oxide, the conductive gate having an upper surface below the upper surface of the substrate;

providing a self-aligned isolation cap on the conductive gate within the trench; and

removing the nitride-containing layer.

28. A field effect transistor structure, comprising:

a substrate with an upper surface, the substrate having a trench therein;

an oxide layer on the bottom and sidewall of the trench;

a conductive layer on the bottom and sidewall of the oxide layer, the conductive layer having an upper surface below the upper surface of the substrate; and

a self-aligned isolation cap on the conductive layer within the trench, the isolation cap comprising a non-organic dielectric material

29. A MOSFET structure, comprising:

a substrate with an upper surface, the substrate having a trench therein;

a source and channel region proximate the trench;

a gate oxide on the bottom and sidewall of the trench;

a conductive gate on the bottom and sidewall of the gate oxide, the conductive gate having an upper surface below the upper surface of the substrate; and

a self-aligned isolation cap on the conductive gate within the trench, the isolation cap comprising a non-organic dielectric material.

30. A semiconductor device containing a field effect transistor structure, the transistor structure comprising:

a substrate with an upper surface, the substrate having a trench therein;

an oxide layer on the bottom and sidewall of the trench;

a conductive layer on the bottom and sidewall of the oxide layer, the conductive layer having an upper surface below the upper surface of the substrate; and

a self-aligned isolation cap on the conductive gate within the trench, the isolation cap comprising a non-organic dielectric material.

31. A semiconductor device containing a MOSFET structure, the MOSFET structure comprising:

a substrate with an upper surface, the substrate having a trench therein;

a source and channel region proximate the trench;

a gate oxide on the bottom and sidewall of the trench;

a conductive gate on the bottom and sidewall of the gate oxide, the conductive gate having an upper surface below the upper surface of the substrate; and

a self-aligned isolation cap on the conductive gate within the trench, the isolation cap comprising a non-organic dielectric material.